Department of Electrical Engineering and Computer Science

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

6.035 Fall 2016

Test II

You have 50 minutes to finish this quiz.

Write your name and athena username on this cover sheet.

Some questions may be harder than others. Read them all through first and attack them in the order that allows you to make the most progress. If you find a question ambiguous, be sure to write down any assumptions you make. Be neat. If we can't understand your answer, we can't give you credit!

This exam is open book and open laptop. Additionally, you may access the course website, but aside from that you may NOT USE THE NETWORK.

Please do not write in the boxes below.

I (xx/20)	II (xx/23)	III (xx/25)	IV (xx/12)	V (xx/20)	Total (xx/100)

Name:

Athena username:

I Register Allocation

In this problem, you will perform register allocation for the following code. Each instruction is labeled with a number. Assume that you do not perform any other optimizations, and none of the variables is subsequently used.

```
    int a, b, c, d;
1:  a = read_int();
2:  b = read_int();
3:  while (a > b) {
4:    c = a - 5;
5:    if (c > b) {
6:      d = c - 1;
7:      a = d + a;
      } else {
8:      d = c + 1;
9:      a = d + a;
      }
10:   b = a - c;
    }
11: print(a);
```

1. [5 points]: Write the set of def-use chains for each variable in the program. Write each def-use chain as number pair (d, u) where d is the label of an instruction that defines the variable and u is the label of an instruction that uses that definition.

a:

b:

c:

d:

2. [5 points]: Write the set of webs in the program. Write each web as the set of instructions that belong to the web. We have given you names `w1-w7` for the webs, use only as many names as you need.

`w1`:

`w2`:

`w3`:

`w4`:

`w5`:

`w6`:

`w7`:

3. [5 points]: Draw the interference graph for the webs. Each node in the interference graph should represent one web. There should be an edge between two nodes if the two webs interfere. Label each node with the name (`w1-w7`) of the corresponding web.

4. [5 points]: Suppose that the architecture we are targeting for compilation has three general purpose registers. Can we place all the variables in this code in registers (ignore any constraint due to calling convention)? If yes, describe an assignment of variables to registers. If no, explain the reason using your interference graph as part of your justification.

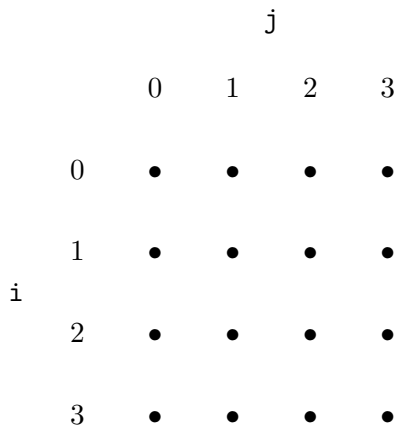
II Parallelization

Consider the following program:

```
for (i = 0; i < n; i += 1) {
  for (j = 0; j < n; j += 1) {
    A[i,j] = A[i - 1, j - 2] + 3;
  }
}
```

`A[i, j]` means the element at the `i`-th row and `j`-th column in the 2-dimensional array `A`. Ignore out-of-bound array access.

5. [3 points]: Assume that `n = 4`. In the grid below, circle the dots that represent the iteration space for this loop. Ignore out-of-range cases. Each dot represents the values of `i` and `j` for an iteration.



6. [5 points]: What is the distance vector for these loops?

7. [5 points]: Without any other optimizations or transformations, is either loop fully parallelizable as a "FORALL" loop? If so, is it the outer loop (i), the inner loop (j), or both, that can be parallelized?

For programs with a sequential portion T_s and a parallelizable portion T_p running on a machine with n processors, recall Amdahl's law and the definition of speedup:

$$T(n) = T_s + \frac{T_p}{n}$$

$$\text{speedup} = \frac{T(1)}{T(n)}$$

Consider a program where 20% of the operations are sequential and 80% are parallelizable.

8. [4 points]: Assume the program runs on a machine with 8 processors, what is the speedup?

9. [6 points]: Regardless of the number of processors in the machine, what is the maximum possible speedup for this computation?

III Dataflow Analysis

Your task in this problem is to design a dataflow analysis that will determine whether each variable $v_1, ..., v_k$ is odd or even at each point in the program. The program itself will be represented as a control flow graph with two kinds of assignment statements:

- $v = c$: sets a variable v to a constant c.
- $v_1 = v_2 + v_3$: sets a variable v_1 to the sum of variables v_2 and v_3.

10. [5 points]: Design the lattice for this dataflow analysis problem. You should specify the set S of lattice elements and the least upper bound operator $\vee$ over the set of lattice elements. We are expecting each lattice element to record an abstract value for each variable $v_1, ..., v_k$. As part of your definition you should define the set of abstract values.

11. [5 points]: Specify the transfer function for each kind of assignment statement. Specifically, specify the transfer function f_n when the control flow graph node n is of the form $n : v = c$ and when n is of the form $n : v_1 = v_2 + v_3$. As part of the solution to this problem we are expecting you to define a version of + that operates on the abstract values.

12. [5 points]: Give the abstraction function $AF(x)$ (here x is a program state of the form $[v_1 \rightarrow c_1, ..., v_k \rightarrow c_k]$ that specifies a value c_i for each variable v_i).

13. [5 points]: Give a program, in the form of a control-flow graph, for which the **meet over all paths** solution to the odd/even analysis problem does not equal the solution that the dataflow analysis algorithm produces. If no such program exists, explain why it does not exist.

14. [5 points]: Give a program, in the form of a control-flow graph, that has **multiple fixed-point** solutions to the dataflow equations that your analysis generates. For this program, provide at least two of the multiple fixed-point solutions. If no such program exists, explain why it does exist.

IV Lattices

You are working with the reaching definitions lattice. Recall that the elements of this lattice are sets of definitions, with each set represented as a bit vector with one position for each definition. Also recall that the order is $x \leq y$ if $x \subseteq y$ and the least upper bound operator is $x \vee y = x \cup y$.

Your teammate comes to you with a set of transfer functions that includes the transfer function $f(x) =$ bitwise not x. In other words, $f(x)$ flips all of the bits in x so that $f(1011) = 0100$ (for example).

15. [6 points]: Is $f(x)$ monotone? Why or why not?

16. [6 points]: Is $f(x)$ distributive? Why or why not?

V Loop Optimizations

In the following program, `j` is a derived induction variable in the family of the base induction variable `i`.

```
i = 0;
while (i < 7) {
  j = i * 4 + 10;
  sum = sum + j;
  i = i + 1;
}
```

17. [10 points]: Rewrite the program after induction variable recognition and induction variable strength reduction (and no other optimizations):

18. [10 points]: Rewrite the program after induction variable recognition, induction variable strength reduction, and induction variable elimination (and no other optimizations):