Loop Optimizations

Instruction Scheduling
Outline

• Scheduling for loops
• Loop unrolling
• Software pipelining
• Interaction with register allocation
• Hardware vs. Compiler
• Induction Variable Recognition
• loop invariant code motion
Scheduling Loops

• Loop bodies are small
• But, lot of time is spend in loops due to large number of iterations
• Need better ways to schedule loops
Loop Example

• Machine
  – One load/store unit
    • load 2 cycles
    • store 2 cycles
  – Two arithmetic units
    • add 2 cycles
    • branch 2 cycles
    • multiply 3 cycles
  – Both units are pipelined (initiate one op each cycle)

• Source Code

\[
\text{for } i = 1 \text{ to } N \\
A[i] = A[i] \times b
\]
Loop Example

• Source Code

```
for i = 1 to N
```

• Assembly Code

```
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```
Loop Example

- Assembly Code

```assembly
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```

Diagram:
```
  d=7
  ↓
  d=5
  ↓
  d=2
  ↓
  d=2
  ↓
  d=2
  ↓
  d=0
```
Loop Example

- **Assembly Code**
  
  ```
  loop:
  mov (%rdi,%rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi,%rax)
  sub $4, %rax
  jz  loop
  ```

- **Schedule (9 cycles per iteration)**

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Outline

- Scheduling for loops
- Loop unrolling
- Software pipelining
- Interaction with register allocation
- Hardware vs. Compiler
- Induction Variable Recognition
- loop invariant code motion
Loop Unrolling

• Unroll the loop body few times
• Pros:
  – Create a much larger basic block for the body
  – Eliminate few loop bounds checks
• Cons:
  – Much larger program
  – Setup code (# of iterations < unroll factor)
  – beginning and end of the schedule can still have unused slots
Loop Example

```
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```
Loop Example

loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
Loop Example

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loop:
  mov    (%rdi,%rax), %r10
  imul   %r11, %r10
  mov    %r10, (%rdi,%rax)
  sub    $4, %rax
  mov    (%rdi,%rax), %r10
  imul   %r11, %r10
  mov    %r10, (%rdi,%rax)
  sub    $4, %rax
  jz     loop
```

- Schedule (8 cycles per iteration)
Loop Unrolling

- Rename registers
  - Use different registers in different iterations
Loop Example

loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
Loop Example

```assembly
loop:
mov (%rdi,%rax), %r10
imul %r11, %r10
mov %r10, (%rdi,%rax)
sub $4, %rax
mov (%rdi,%rax), %rcx
imul %r11, %rcx
mov %rcx, (%rdi,%rax)
sub $4, %rax
jz loop
```
Loop Unrolling

- Rename registers
  - Use different registers in different iterations

- Eliminate unnecessary dependencies
  - again, use more registers to eliminate true, anti and output dependencies
  - eliminate dependent-chains of calculations when possible
Loop Example

loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    mov (%rdi,%rax), %rcx
    imul %r11, %rcx
    mov %rcx, (%rdi,%rax)
    sub $4, %rax
    jz loop
loop:
  mov  (%rdi, %rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi, %rax)
  sub $8, %rax
  mov  (%rdi, %rbx), %rcx
  imul %r11, %rcx
  mov %rcx, (%rdi, %rbx)
  sub $8, %rbx
  jz   loop
Loop Example

loop:

\[
\begin{align*}
\text{mov} & \quad (\%rdi,\%rax), \quad \%r10 \\
\text{imul} & \quad \%r11, \quad \%r10 \\
\text{mov} & \quad \%r10, \quad (\%rdi,\%rax) \\
\text{sub} & \quad $8, \quad \%rax \\
\text{mov} & \quad (\%rdi,\%rbx), \quad \%rcx \\
\text{imul} & \quad \%r11, \quad \%rcx \\
\text{mov} & \quad \%rcx, \quad (\%rdi,\%rbx) \\
\text{sub} & \quad $8, \quad \%rbx \\
\text{jz} & \quad \text{loop}
\end{align*}
\]

• Schedule (4.5 cycles per iteration)
Outline

• Scheduling for loops
• Loop unrolling
• **Software pipelining**
• Interaction with register allocation
• Hardware vs. Compiler
• loop invariant code motion
• Induction Variable Recognition
Software Pipelining

- Try to overlap multiple iterations so that the slots will be filled
- Find the steady-state window so that:
  - all the instructions of the loop body is executed
  - but from different iterations
## Loop Example

- **Assembly Code**
  ```
  loop:
  mov (%rdi,%rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi,%rax)
  sub $4, %rax
  jz loop
  ```

- **Schedule**

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Loop Example

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loop:
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Loop Example

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<td>sub1</td>
<td>sub2</td>
<td>sub</td>
<td>sub3</td>
<td>sub2</td>
<td>sub3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
Loop Example

- **Assembly Code**
  ```assembly
  loop:  
    mov (%rdi,%rax), %r10 
    imul %r11, %r10 
    mov %r10, (%rdi,%rax) 
    sub $4, %rax 
    jz  loop
  ```

- **Schedule (2 cycles per iteration)**
Loop Example

• 4 iterations are overlapped
  – value of %r11 don’t change
  – 4 regs for (%rdi, %rax)
  – each addr. incremented by 4*4
  – 4 regs to keep value %r10
  – Same registers can be reused after 4 of these blocks
generate code for 4 blocks, otherwise need to move

```
loop:
  mov (%rdi, %rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi, %rax)
  sub $4, %rax
  jz loop
```

<table>
<thead>
<tr>
<th>mov4</th>
<th>mov2</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov1</td>
<td>mov4</td>
</tr>
<tr>
<td>mul3</td>
<td>jz1</td>
</tr>
<tr>
<td>jz</td>
<td>mul3</td>
</tr>
<tr>
<td>mul2</td>
<td>sub2</td>
</tr>
<tr>
<td>sub1</td>
<td></td>
</tr>
</tbody>
</table>
Software Pipelining

- Optimal use of resources
- Need a lot of registers
  - Values in multiple iterations need to be kept
- Issues in dependencies
  - Executing a store instruction in an iteration before branch instruction is executed for a previous iteration (writing when it should not have)
  - Loads and stores are issued out-of-order (need to figure-out dependencies before doing this)
- Code generation issues
  - Generate pre-amble and post-amble code
  - Multiple blocks so no register copy is needed
Outline

- Scheduling for loops
- Loop unrolling
- Software pipelining
- *Interaction with register allocation*
- Hardware vs. Compiler
- Induction Variable Recognition
- loop invariant code motion
Register Allocation and Instruction Scheduling

- If register allocation is before instruction scheduling
  - restricts the choices for scheduling
Example

1: mov 4(%rbp), %rax
2: add %rax, %rbx
3: mov 8(%rbp), %rax
4: add %rax, %rcx
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Anti-dependence
How about a different register?
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Register Allocation and Instruction Scheduling

- If register allocation is before instruction scheduling
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- If instruction scheduling is before register allocation
  - Register allocation may spill registers
  - Will change the carefully done schedule!!!
Outline

• Scheduling for loops
• Loop unrolling
• Software pipelining
• Interaction with register allocation
• **Hardware vs. Compiler**
• Induction Variable Recognition
• loop invariant code motion
Superscalar: Where have all the transistors gone?

• Out of order execution
  – If an instruction stalls, go beyond that and start executing non-dependent instructions
  – Pros:
    • Hardware scheduling
    • Tolerates unpredictable latencies
  – Cons:
    • Instruction window is small
Superscalar: Where have all the transistors gone?

• Register renaming
  – If there is an anti or output dependency of a register that stalls the pipeline, use a different hardware register
  – Pros:
    • Avoids anti and output dependencies
  – Cons:
    • Cannot do more complex transformations to eliminate dependencies
Hardware vs. Compiler

• In a superscalar, hardware and compiler scheduling can work hand-in-hand
• Hardware can reduce the burden when not predictable by the compiler
• Compiler can still greatly enhance the performance
  – Large instruction window for scheduling
  – Many program transformations that increase parallelism
• Compiler is even more critical when no hardware support
  – VLIW machines (Itanium, DSPs)